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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,485	03/22/2004	Michael R. Lambert	10030245-1	2796

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EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,485	LAMBERT ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *1,13,14,16,19 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/22/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 are present for examination.

Priority

Acknowledgement is made that no priority either foreign or domestic is claimed for this application and as such the filing date (3/22/2004) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that an Information Disclosure Statement (IDS) was provided with the application and has been fully considered.

Drawings

The drawings are not objected to at this time since examiner does not see any problems or informalities at this time with the drawings as they are.

Claim Objections

Claim 1 is objected to because of the following informalities:

There is lacking a ":" at the end of line 5 of the claim.

Appropriate correction is required for overcoming this objection.

Claim 13 is objected to because of the following informalities:

"an model" in line 4 of the claim should read "a model" to be proper.

There is a lacking ":" at the end of line 4 of the claim.

Appropriate correction is required for overcoming this objection.

Claim 14 is objected to because of the following informalities:

There is improper punctuation "," in lines 6, 7, and 9 of the came.

Appropriate correction is required for overcoming this objection. Examiner recommends replacing each "," with the correct ";" to overcome this objection.

Claim 16 is objected to because of the following informalities:

"an model" in line 8 of the claim should read "a model" to be proper.

There is a lacing ":" at the end of lines 4 and 8 of the claim.

Appropriate correction is required for overcoming this objection

Claim 21 is objected to because of the following informalities:

"an model" in line 2 of the claim should read "a model" to be proper.

Appropriate correction is required for overcoming this objection.

Claim 19 is objected to because of the following informalities:

There is a lacking ":" at the end of line 5 of the claim.

Appropriate correction is required for overcoming this objection.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. Claim 1 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. This claim appears to be solely software, which lacks the ability to produce a useful, concrete and tangible result and as such is rejected under 35 U.S.C. 101. Appropriate correction is required to overcome this rejection

2. Claims 2-12 fail to resolve the 35 U.S.C. 101 issue of claim 1 and thus are also rejected under the 35 U.S.C. 101.

3. Claim 13 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. This claim appears to be solely software, which lacks the ability to produce a useful, concrete and tangible result and as such is rejected under 35 U.S.C. 101. Examiner interprets that the "means" would be interpreted by one of ordinary skill in the art as software.

4. Claim 14 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. This claim appears to be solely data, which lacks the ability to produce a useful, concrete and tangible result and as such is rejected under 35 U.S.C. 101. Examiner interprets that the "electronic representation" as simply a data structure. Appropriate correction is required to overcome this rejection.

5. Claim 15 fails to resolve the 35 U.S.C. 101 issue of claim 14 and thus is also rejected under the 35 U.S.C. 101.

6. Claim 16 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. This claim appears to be solely software, which lacks the ability to produce a useful, concrete and tangible result and as such is rejected under 35 U.S.C. 101. Examiner interprets that the "means" and "generator" would be interpreted by one of ordinary skill in the art as software. Appropriate correction is required to overcome this rejection.

7. Claims 17 and 19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. This claim appears to be solely

software, which lacks the ability to produce a useful, concrete and tangible result and as such is rejected under 35 U.S.C. 101. Examiner interprets that the "creating" would be interpreted by one of ordinary skill in the art as a computation within a processor lacking a tangible result. Appropriate correction is required to overcome this rejection.

8. Claims 18 and 20 fail to resolve the 35 U.S.C. 101 issue of claims 17 and 19 respectively and thus is also rejected under the 35 U.S.C. 101.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6-8, 11 and 14-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Whetsel (US 6519729 B1).

9. As per claim 1, Whetsel teaches:

Code for identifying a respective parent portion and any respective branch portions (column 3 lines 53-55, column 4 lines 2-3,and figures 2 and 4 column 6 lines 22-28) of a scan chain of a circuit device, the scan chain having a scan input (SI figures 2 and 4, SI 1-10 figure 7) and one or more scan outputs (S0 figures 2 and 4, SO 1-10 figure 7) and a plurality of scan cells disposed therebetween (figures 2 and 4, and column 3 lines 49-50); and

Code for creating a model (figure 2 and 4) of the scan chain, including;

Code for creating a dummy cell chain which includes creating one or more dummy cells and connecting the one or more dummy cells between the scan input and a branch portion of the scan chain (column 2 lines 55-57).

10. As per claim 2, Whetsel teaches, wherein the process related to testing a circuit device is a process selected from the group consisting of: creating a test, generating a test patter, automatically generating a test pattern, validating a test, verifying a test, setting up a test or running a test (during scan testing - column 1 lines 55-56).

11. As per claim 3, Whetsel teaches, wherein the code for creating a dummy cell chain further includes code selected from the group of:

Code for breaking the branch portion from the parent portion of the scan chain in the model (column 3 lines 46-50);

Code for inserting the one or more dummy cells in the branch chain immediately prior to the existing cells in the branch chain and immediately after the scan input (column 3 lines 55-57);

Code for creating the dummy chain in parallel to the parent chain (column 3 lines 56-57 and figures 2,4, and 7, column 6 lines 40-45); and

Code for creating exactly the same number of dummy cells exactly matching the number of non-branched parent cells in the parent portion of the scan chain (column 3 lines 55-57).

12. As per claim 6, Whetsel teaches, wherein the tool is at least part of a computer program and the code portion thereof are program codes (column 3 lines 41-57 with figures 1 and 2).

13. As per claim 7, Whetsel teaches, wherein the tool is at least partly comprising of hardware (figures 1, 2, and 4).

14. As per claim 8, Whetsel teaches, wherein the circuit device is selected from the group consisting of an IC device and a circuit board (column 1 line 25-30).

15. As per claim 11, Whetsel teaches, wherein the tool forms a part of apparatus selected from the group consisting of: test equipment; or automated test equipment; or computer equipment for test pattern generation or validation (figure 2 and 4).

16. As per claim 14, Whetsel teaches:

An electronic representation of a branched scan chain of the circuit device, the branched scan chain having scan cells in a parent portion and a branch portion, the branch portion branching off the parent portion (figures 1, 2, and 4, column 3 lines 45-50);

Whereby the electronic representation includes:

A representative parent portion of scan cells (figure 2 and column 3 lines 53-54, column 4 lines 2-3, and figures 2 and 4), and

A branch dummy portion of scan cells (figure 2 and 4, column 3 lines 55-57),

Whereby the representative parent portion is an electronic representative of the scan cells of the parent portion of the branched scan chain of the circuit device (figures 2 and 4), and

Whereby the branched dummy portion includes;

An electronic representative of the scan cells of the branched portion of the branched scan chain of the circuit device (figures 2 and 4); and

One or more dummy scan cells disposed prior to the electronic representative scan cells of the branched portion of the branched scan chain, and whereby the dummy scan cells are connected to the electronic representative of the scan cells of the branched portion of the branched scan chain, such that the dummy scan cells are disposed to communicate therewith (column 3 lines 55-57, figures 2 and 4).

17. As per claim 15, Whetsel teaches, wherein the tool is an abstract software model of the circuit device used with apparatus selected from the group consisting: of test equipment; automated test equipment; and computer equipment for test pattern generation or validation (figures 2 and 4, column 2 lines 40-43, column 1 lines 55-56).

18. As per claim 16, Whetsel teaches, A system for setting up a test for a circuit device comprising:

A test pattern generator which receives input relative to a circuit device to be tested and which outputs a test patter for testing the circuit device (figures 1, 2, and 4, column 2 lines 40-43);

A tool which operates with a test pattern generator, the tool having

Means for identifying respective parent and branch portions of a scan chain of a circuit device (column 3 lines 53-55, column 4 lines 2-3, and figures 2 and 4), the scan chain having a scan input and a plurality of scan outputs and a plurality of scan cells (figures 2 and 4, column 3 lines 58-60);

Means for creating an model of the scan chain (figures 2 and 4), including

Means for creating a dummy cell chain which includes the branch portion of the scan chain connected with one or more dummy cells and the scan input (column 3 lines 54-57).

19. As per claim 17, Whetsel teaches:

Identifying respective parent and branch portions of a scan chain of the device (column 3 lines 53-55, column 4 lines 2-3, and figures 2 and 4), the scan chain having a plurality of scan cells and at least one scan input and a plurality of scan outputs (figures 2 and 4, column 3 lines 53-57); and

Creating a model of the scan chain, the model comprising the parent portion of the scan chain, and dummy cells connected between the scan input and the branch of the scan chain (figures 2 and 4).

20. As per claim 18, Whetsel teaches, wherein said creating a model further comprises:

Disconnecting the branch from the parent (figures 2 and 4).

21. As per claim 19, Whetsel teaches:

Identifying respective parent and branch portions of an actual scan chain of a circuit device (column 3 lines 53-55, column 4 lines 2-3,and figures 2 and 4), the actual scan chain having a plurality of scan cells and at least one scan input and a plurality of scan outputs (figure 1); and

Creating a model of the scan chain (figures 2 and 4), including

Creating a dummy cell chain which includes the branch portion of the scan chain connected with one or more dummy cells and the scan input (column 3 lines 55-57 and figures 2 and 4).

22. As per claim 20, Whetsel teaches, wherein the test-related process is a process selected from the group consisting of: creating a test, generating a test pattern, automatically generating a test pattern, validating a test, verifying a test, setting up a test or running a test (column 1 lines 26-27, column 2 lines 40-43, figures 2 and 4).

23. As per claim 21, Whetsel teaches:

Using an model of a scan chain of a circuit device, including a parent portion and a dummy cell portion of the respective chain, the dummy cell portion including the branch portion of the scan chain connected with one or more dummy cells and the common scan input which is in common with the parent portion (figures 2 and 4, column 3 lines 53-57, column 4 lines 2-3);

Shifting test bits into the common scan input (column 4 lines 14-31);

Populating the parent and the dummy portions of the model which includes populating the branch portion of the scan chain (column 4 lines 14-31); and

Capturing a response to the test bits shifted into the scan input (column 2 lines 40-43).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 4, 5, 9, 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel (US 6519729 B1).

24. As per claim 4, Whetsel teaches the above as per claim 1, wherein a parent portion and branch portion of a scan chain having one or more outputs are identified and additional dummy cells are added to equalize the lengths of the identified portions.

Whetsel does not specifically teach wherein claim 1 further including code for preliminarily determining whether the scan chain has a plurality of outputs.

However Examiner interprets the only way to accurately and fully test or examine a scan chain all outputs thereof of the scan chain must be known and thus determined prior to testing or examination of the scan chain.

Therefore one of ordinary skill in the art at the time the invention was made would recognize that any and all systems performing such procedures such as testing or examining circuitry must preliminarily determine whether a scan chain has a plurality of outputs.

25. As per claim 5, Whetsel teaches the above as per claim 1, wherein a parent portion and branch portion of a scan chain having one or more outputs are identified and additional dummy cells are added to equalize the lengths of the identified portions.

Whetsel does not specifically teach wherein claim 1 further including code selected from the group of code for determining whether there remain any branch portions of the scan chain for which a dummy cell chain may be created; and

Code for determining whether there remain any branch portions off another branch portion of the scan chain for which a dummy cell chain may be created.

However Examiner interprets that wherein Whetsel teaches that a number of branches (three - column 6 line 24) may exist in combination with equalizing the lengths of each scan path (column 3 line 56), a determination must be made as to whether a dummy cell chain may be created or required for all branches.

Therefore one of ordinary skill in the art at the time the invention was made would recognize that all branches within a scan chain would need to be examined so that a dummy cell chain may be created when required to equalize the lengths of the scan path.

26. As per claims 9, 10, and 12, Whetsel teaches the above as per claim 1, wherein a parent portion and branch portion of a scan chain having one or more outputs are identified and additional dummy cells are added to equalize the lengths of the identified portions.

Whetsel does not specifically teach wherein the model is communicated to circuit test equipment for use during testing of the circuit device.

However Examiner interprets that the model must be communicated since without the model the circuit test equipment could not perform testing on the scan paths.

Therefore one of ordinary skill in the art at the time the invention was made would recognize that any model would be required to be communicated to circuit test equipment in order to perform testing on the scan paths modeled.

27. As per claim 13, Whetsel teaches:

Means for identifying respective parent and branch portions of a scan chain of the device (column 3 lines 53-57, column 4 lines 2-3, figures 2 and 4); and

Means for creating an model of the scan chain (figures 2 and 4), including

Means for breaking the branch portion from the parent portion of the scan chain in the model (figures 2 and 4, column 3 lines 41-50);

Means for inserting one or more dummy cells in the branch chain prior to the existing cells in the branch chain (column 3 lines 53-57, figures 2 and 4).

Whetsel does not specifically teach:

Means for re-connecting the branch chain with the inserted dummy cells to the scan input in the model of the scan chain.

However Whetsel's teachings are related to testing in a scan test mode not in the functional operation or normal mode of operation for a device therein the scan chain resides which the device must be able to return to.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to re-connect the branch chain with the inserted dummy cells to the scan input in the model of the scan chain in order to return to functional operation or normal mode of operation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven D. Radosevich
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER